Abstract of the Disclosure

The present invention provides a manufacturing method of a semiconductor device, in which an oxide layer for regulating the ion-implantation is previously formed before the implantation of the impurities into a predetermined region of a P-lightly doped drain (LDD) to optionally regulate the implantation state of P type impurities into the corresponding predetermined region of P-LDD based on the oxide layer for regulating the ion-implantation so that the PMOS side predetermined channel length is elongated longer than the NMOS side predetermined channel length, thus maintaining the finished PMOS and NMOS side channel lengths equal irrespective of diffusion velocity of the impurities even if a substantial annealing process is performed and P type impurities are diffused faster than N type impurities due to their structural difference.

When the PMOS and NMOS side channel lengths are maintained equal irrespective of diffusion velocity of the respective impurities, the finished PMOS device and the finished NMOS device will have the same threshold voltage, maintaining the quality of a high integrated semiconductor device over a certain level.

Also, the present invention provides a method of manufacturing a semiconductor device, wherein separate spacers are selected and formed on a different scales before

the implantation of the impurities into the predetermined regions of a P-lightly doped drain (LDD) and an N-LDD to optionally regulate the implantation state of impurities into the respective predetermined regions of the LDD based on the differently scaled spacers so that, if necessary, the PMOS and NMOS side predetermined channel lengths are selectively regulated, thus, if necessary, effectively regulating the finished PMOS and NMOS side channel lengths irrespective of diffusion velocity of the respective impurities even if a substantial annealing process is performed and P type impurities are diffused faster than N type impurities due to their structural difference.

When the PMOS and NMOS side channel lengths are maintained at a desired effective value irrespective of diffusion velocity of the respective impurities, the finished PMOS device and the finished NMOS device will have the desired threshold voltage, easily maintaining the quality of a high integrated semiconductor device over a certain level.